

University of Toronto
Department of Electrical and Computer Engineering

ECE 342 - Digital Hardware

Final Examination

February 2000

Last Name: _____

First Name: _____

Student Number: _____

Signature: _____

Duration: **2 Hours**

Answer ALL questions on this test paper. There is extra space at the end if you need it.

EXAMINER'S REPORT

1 _____ /10

2 _____ /15

3 _____ /10

4 _____ /15

5 _____ /15

6 _____ /10

7 _____ /15

TOTAL: _____ /90

Question 1 — [10 marks]

a. Give an example of two k -cubes A, B such that:

i. $A * B$ yields a smaller cube: $A = \underline{\hspace{2cm}}$, $B = \underline{\hspace{2cm}}$

ii $A * B$ yields a larger cube: $A = \underline{\hspace{2cm}}$, $B = \underline{\hspace{2cm}}$

iii $A * B$ yields a k -cube: $A = \underline{\hspace{2cm}}$, $B = \underline{\hspace{2cm}}$

b. Given

$$C^{k+1} = \{0x1, x01, x11, 1x1, 11x\} \text{ and}$$

$$G^{k+2} = \{001, 011, xx1, x11, 101, 1x1, 111\}$$

Evaluate the following:

$$C^{k+2} = \{C^{k+1} \cup G^{k+2} - (\text{redundant cubes})\}$$

$$C^{k+2} = \underline{\hspace{10cm}}$$

c. For some function, f , we use the initial cover $C^0 = ON \cup DC$ and then generate the prime implicants. Assume that to check if some PI, p^i , is essential, we use the following test:

$$p^i \# (C - p^i) \# \{DC - p^i\} \neq \phi ?$$

then under what conditions will this test produce a wrong result?

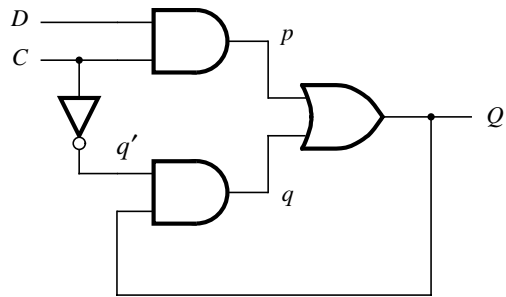
Answer: _____

d. Two rows of a Flow Table can be merged into a single row (thus reducing the number of states by 1) if their next state entries in all columns are compatible. They are compatible if the next state entries are either 1. the same, or 2. one or both is unspecified, or 3. both are stable. With respect to 3. (both are stable) what additional requirement (besides compatible next state entries) is implied?

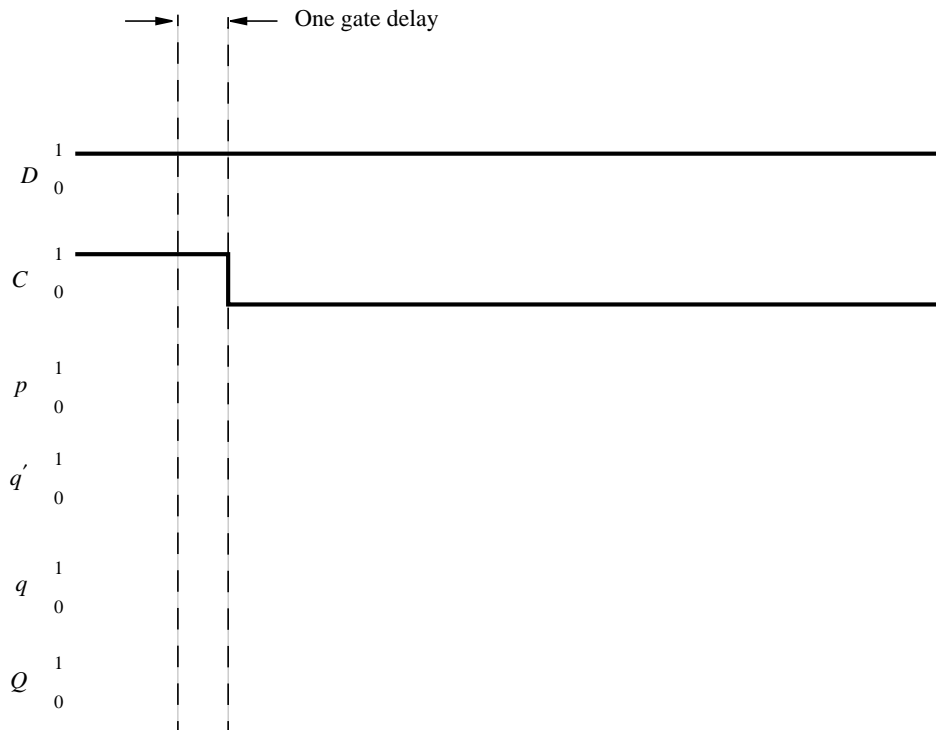
Answer: _____

Question 2 — [15 marks]

a Consider the circuit below:



Assuming the delay through each gate is *exactly* the same (non-zero), complete the timing diagram below:



- b The following Excitation Table describes an asynchronous arbiter for two devices, for which the grant signals are active low. Give a circuit that implements this arbiter using only the following logic gates: four 2-input NAND gates and 1 NOT gate.

PS y_2y_1	NS Y_2Y_1				Outputs g_2g_1
	$r_2r_1 = 00$	01	10	11	
00	00	01	10	01	11
01	00	01	10	01	10
10	00	01	10	10	01
11	-	01	10	-	dd

DRAW THE CIRCUIT IN THE SPACE BELOW:

Question 3 — [10 marks]

For a function, f , consider the following cover:

$$f(x_1, x_2, x_3, x_4, x_5) = \{0x00x0, 0x001x, 0x000x, 01x111, 100011\}$$

- a** Below, list the prime implicants of f . You must derive your answers in the space on the next page using the procedure discussed in class; specifically, you must use the procedure in which the original cover (given above) is called C^0 and you generate a new cover $C^1 = G^1 \cup C^0 - (\text{redundant cubes})$, and so on until the prime implicants are generated.

List the prime implicants below and derive them in the space given on the following page.

Prime implicants: _____

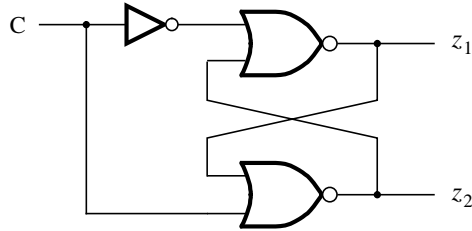
List the essential prime implicants (you do not have to show your work for

this part): _____

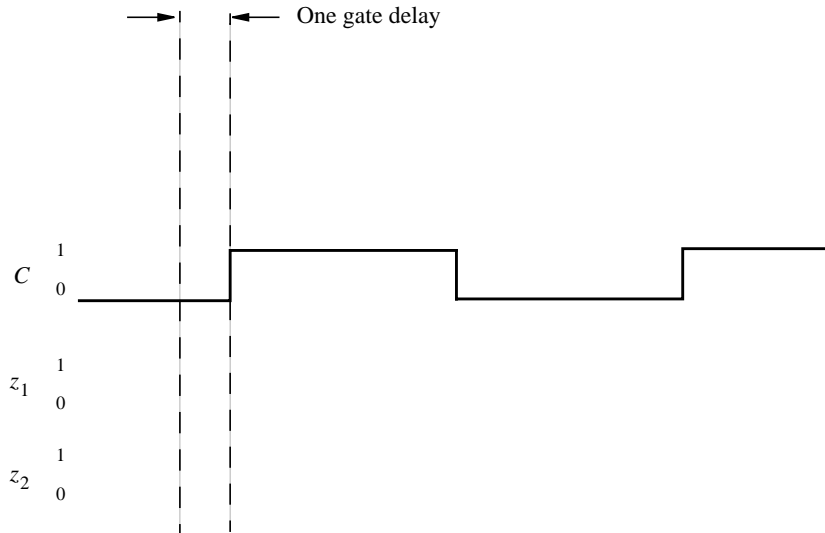
ANSWER SPACE FOR DERIVING THE PRIME IMPLICANTS

Question 4 — [15 marks]

a Consider the sequential circuit:



Complete the following timing diagram. Assume that all gate delays are *equal*:



Assume that we wish to model the above circuit as an asynchronous FSM, in which the present state, y , is represented by the output of the top NOR gate (which is also z_1). In the space on the next page give an Excitation Table that represents the circuit as a Mealy machine with the input C and the outputs $z_1 z_2$.

ANSWER SPACE FOR DRAWING THE Excitation Table

- e. When performing state assignment for asynchronous FSMs, what is the purpose of using the Transition Diagram concept discussed in class?

Answer: _____

Question 5 — [15 marks]

Given the following Flow Table:

PS	NS				z
	$x_1x_2 = 00$	01	10	11	
A	Ⓐ	B	C	-	0
B	A	Ⓑ	-	F	0
C	A	-	Ⓒ	F	0
D	Ⓓ	E	C	-	1
E	D	Ⓔ	-	F	0
F	-	E	C	Ⓕ	1

Show below a Merger Diagram that indicates compatible states for merging if the Moore Model is preserved:

Show below a Merger Diagram that indicates compatible states for merging if the Mealy Model is allowed:

Assuming the machine will be changed to the Mealy model, show below the modified Flow Table (without yet merging any rows):

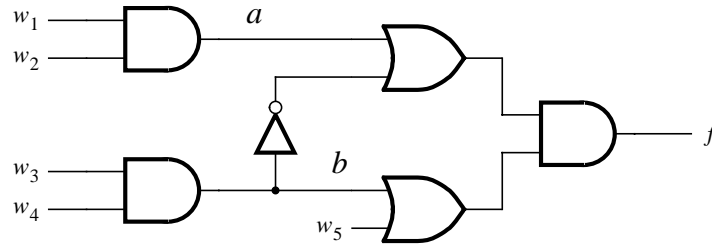
Show below the reduced Flow Table that has the minimum number of states achievable through merging:

In general, which step should be done first when attempting to merge rows of a Flow Table?

Circle: Redraw Flow Table as Mealy Draw Merger Diagram

Question 6 — [10 marks]

a For the circuit



i. If we wish to test whether the fault $a/0$ is present, give a test that propagates this fault to the output, f .

ANSWER: _____

ii. If we wish to test whether the fault $b/0$ is present, give a test that propagates this fault to the output, f .

ANSWER: _____

b Give a test that distinguishes between two circuits that implement the following expressions:

$$f = x_1x_2x_3 + x_2\bar{x}_3x_4 + \bar{x}_1\bar{x}_2x_4 + \bar{x}_1x_3\bar{x}_4$$

$$g = (\bar{x}_1 + x_2)(x_3 + x_4)$$

ANSWER: _____

Question 7 — [15 marks]

a As you have seen in the Lab experiments, DTACK is one of the control signals of any 68K microprocessor based system. Answer the following questions about it:

i. Is it an input signal to the processor or an output signal from it?

ANSWER: _____

ii. When is it asserted and by who (which device(s))?

ANSWER:

iii. What does it mean when it is asserted?

ANSWER:

iv. What does it mean when it is unasserted?

ANSWER:

b i. In Lab # 3 (processor) what is the signal master68k used for?

ANSWER:

ii. Who controls the signal?

ANSWER:

iii. How did you test your SRAM controller once you programmed the FPGA? Say what you expected it to do and how you tested it. How thorough was your test? Did it have any limitations?

ANSWER:

- c Design a state machine to control a hardware device that can be used to initialize a portion of memory. The hardware device (a simple DMA controller) sits on the 68000 bus and will be implemented in an FPGA. You may assume that the memory being initialized always begins at address \$40000.

The hardware device has two memory-mapped 16-bit registers that must be written to by the processor before the device can start. The first register, called count, contains the number of words to be initialized. The second register, called init, contains the value to which to initialize the memory locations. The init register is tri-stated and controlled by a signal called init_oe.

The device also contains a 15-bit counter which increments after each write is performed. The tri-stated output of the counter is connected to address lines 15-1 on the bus and used to generate the address of the location being written. The counter value is driven to the bus by asserting a signal called counter_oe. The upper 8 bits of the address, 23-16, are driven to the bus by asserting a signal called addr_oe. Both counter_oe and addr_oe must be asserted to generate a valid address.

A switch is used to start the hardware device. Turning on the switch sets a signal called start to '1'. When the counter output is equal to the value in the register "count", a signal called done_count is asserted. You are **only required to draw an ASM chart** for the state machine to control the device and need not worry about the circuits to control the initialization of the registers or the counter described above. The state machine will sit idle until the start signal is asserted. The inputs to the state machine are: start, done_count, bg, dtack. The outputs the are: br, count_oe, init_oe, rw, addr_oe. The bidirectional signals are: bgack, as, uds, lds.

PUT YOUR ANSWER ON THE NEXT PAGE

ANSWER SPACE FOR DERIVING THE ASM Chart

EXTRA SPACE — USE ONLY IF NEEDED

EXTRA SPACE — USE ONLY IF NEEDED

EXTRA SPACE — USE ONLY IF NEEDED