

SOLUTION – ECE342 – Midterm - de

Question 3 – [15 marks]

You are to design the circuit represented in Figure 1, which includes

- one 8-bit input register A, which contains a 2's complement signed number $A \{a7...a0\}$
- a FSM
- one 8-bit output register S, which contains a 2 complement signed number $\{s7...s0\}$

The FSM is used for a serial implementation of the operation $S = -A$ (negation)

Hint: The 2' complement of a number A can be computed as the 1's complement +1

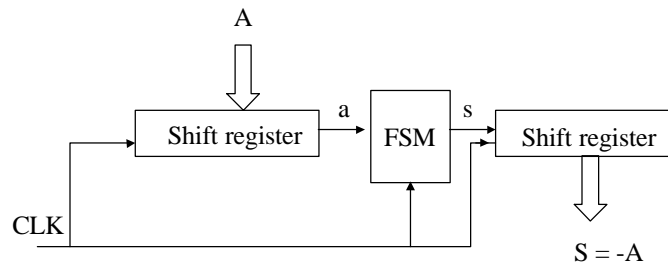
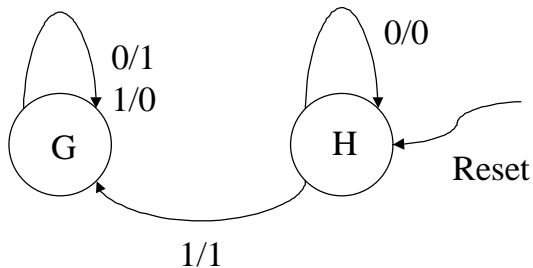


Figure 1

The shift registers have Enable and Load inputs.

- a) Give the state diagram of the Mealy FSM that realizes the serial implementation of the negation operation. [1 mark]



- b) Give the assigned state table of the Mealy FSM and the corresponding equations that are used to implement the FSM.

Use the standard notations : y_i for present states, Y_i for next states, a for the input and s for the output.

Assigned state table [1 mark]

	A=0	A=1	A=0	A=1
y	Y	Y	S	S
0	0	0	1	0
1	1	0	0	1

OR

	A=0	A=1	A=0	A=1
y	Y	Y	S	S
0	0	1	0	1
1	1	1	1	0

Equations: [2 marks]

$$Y = \bar{a}.y$$

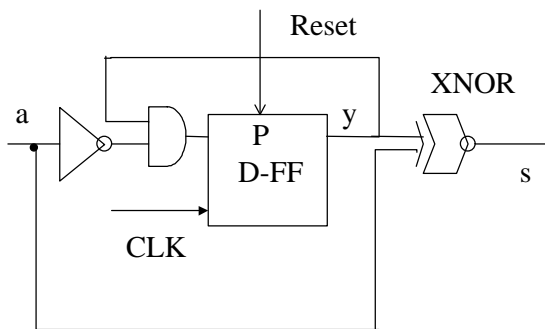
$$s = \bar{a}.\bar{y} + ay = a \odot y$$

OR

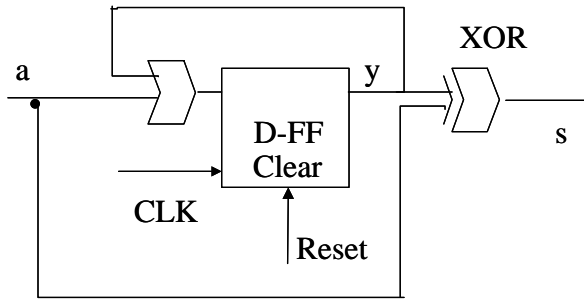
$$Y = y + a$$

$$s = a \text{ xor } y$$

c) Draw the Mealy FSM with D flip-flops (with Preset and Clear asynchronous inputs) and usual gates. [1 mark]

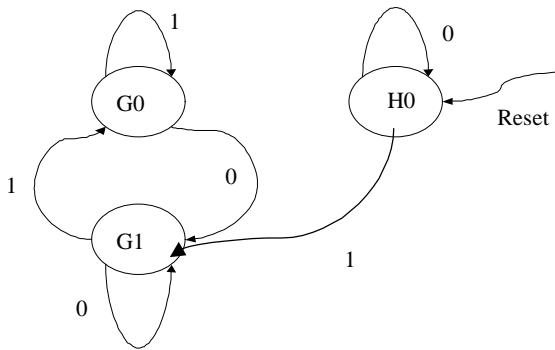


OR



d) Give the state diagram of the Moore FSM that realizes the serial implementation of the negation operation. **[1 mark]**

e) Give the assigned state table of the Moore FSM and the corresponding equations that are used to implement the FSM.



Use the standard notations : y_i for present states, Y_i for next states, a for the input and s for the output.

State assignment table (2 codings)

[1 mark]

		a=0	a=0	a=1	a=1	
y_2	y_1	Y_2	Y_1	Y_2	Y_1	s
0	0	0	1	0	0	0
0	1	0	1	0	0	1
1	0	1	0	0	1	0
1	1	d	d	d	d	d

$$Y_2 = \bar{a}.y_2$$

$$Y_1 = \bar{a}.y_2$$

$$s = y_1$$

[3 marks]

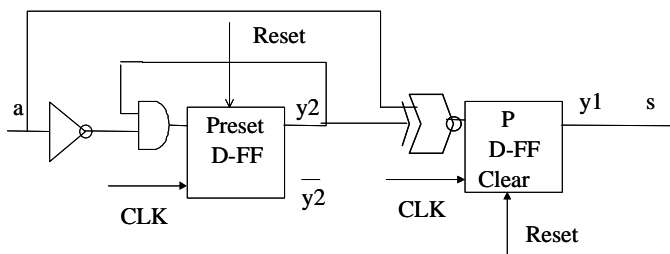
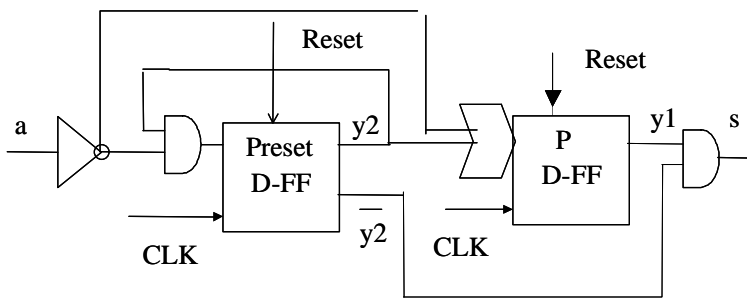
		a=0	a=0	a=1	a=1	
y2	y1	Y2	Y1	Y2	Y1	s
0	0	0	1	0	0	0
0	1	0	1	0	0	1
1	1	1	1	0	1	0
1	0	d	d	d	d	d

$$Y_2 = \bar{a} \cdot y_2$$

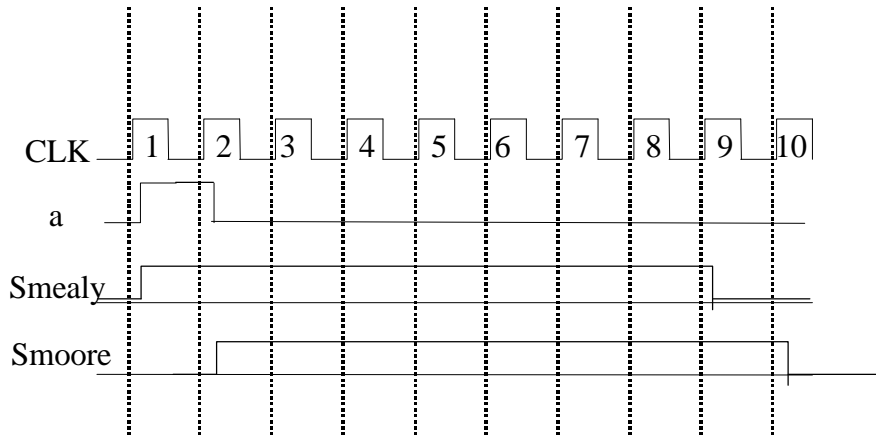
$$Y_1 = \bar{a}$$

$$s = y_2 \cdot y_1$$

f) Draw the Moore FSM with D flip-flops (with Preset and Clear asynchronous inputs) and usual gates. [1 mark]



g) Draw the outputs of the Mealy and Moore FSM corresponding timing diagram below [2 marks]



h) Complete the circuit schematic of Figure 2. The input value is loaded in register A by the reset signal and the output value must be kept in the output register at the end of the operation. [2 marks]

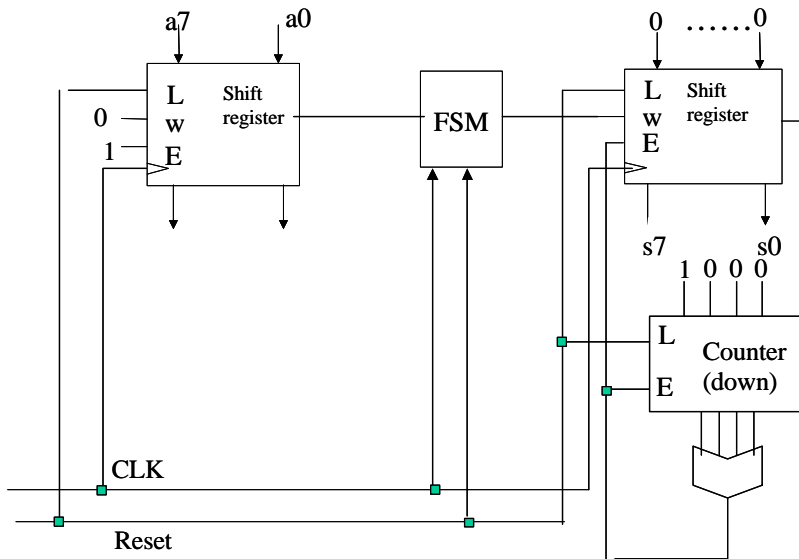


Figure 2

Question 4 [10 marks]

You are to design a circuit that produces the parity check bit of a n -bit word A by using the sequential approach. The parity bit is 1 when the n -bit word has an odd number of 1's. The parity bit is called p .

Write pseudo-code for the operation, using the format given in class. Assume A can be shift to the right. [2 marks for optimal algorithm, 1 mark for non-optimal]

```
p=0;
while A!=0
```

```

{ p = p XOR a0 ;
  A=A/2;
}

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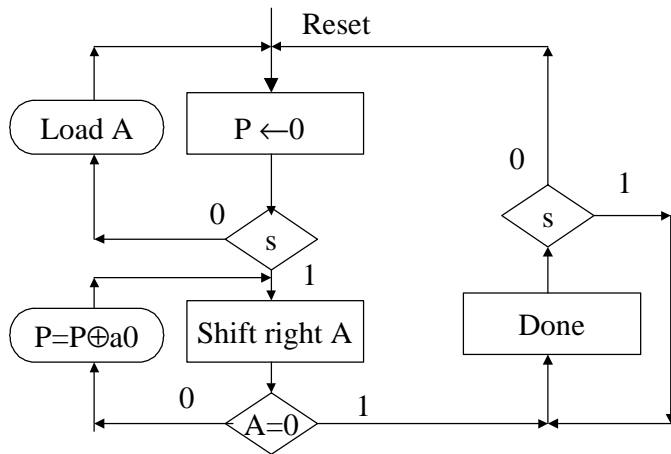
Other (more complex) solution

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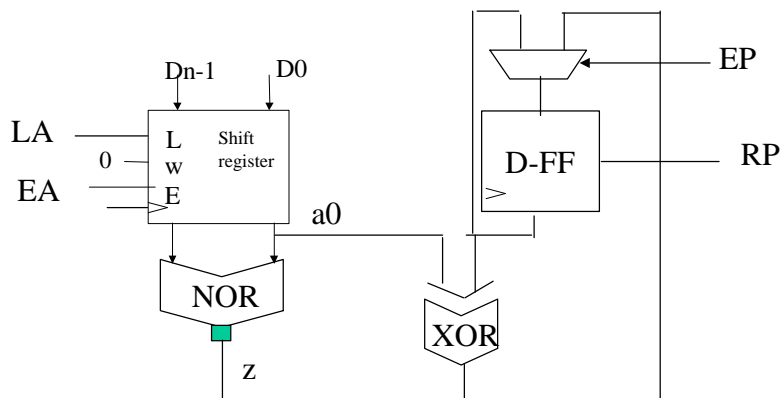
p = 0;
while A != 0
  {
  if (a0 == 1)
    p = NOT (p) ;
  A= A/2 ;
  }

```

Draw an ASM chart that represents your pseudo-code. Assume an externally supplied input *s* is provided and is set to 1 when A has been loaded and the operation should begin. Set an output *Done* to 1 when the operation is complete. [2 marks]



Draw a datapath for your circuit. Label all names with reasonable names: [4 marks]



d) For the control part, what would be the input and output signals? [2 marks]

Input signals: s, z

Output signals: EA, LA, EP, RP, Done