

1) [15] Array multipliers:

a) Draw a gate-level design of a Booth encoder cell. Label the inputs and outputs of the cell as we did for Lab #0.

b) Draw a gate-level design of the general multiplier cell used in a Booth multiplier. You do not need to show the details of the full-adder block.

c) For a 32-bit x 32-bit unsigned multiplier, how many levels are required in a Wallace tree? Show how you found the result. You do not have to show the tree or the connections, but must show the technique you used to find the answer.

d) For a 32-bit x 32-bit Booth multiplier, how many levels are required in a Wallace tree? Show how you found the result. You do not have to show the tree or the connections, but must show the technique you used to find the answer.

e) What would be the result from part e if the multiplier operand were the hexadecimal constant \$760, assuming you wanted to use as few rows as possible? Booth Bit-Pair Recoding is **not** to be done.

f) What is the advantage of Booth Bit-Pair Recoding? (briefly)

g) Can a Wallace tree be used with Booth Bit-Pair Recoding? Explain.

2) [13] Clock circuits

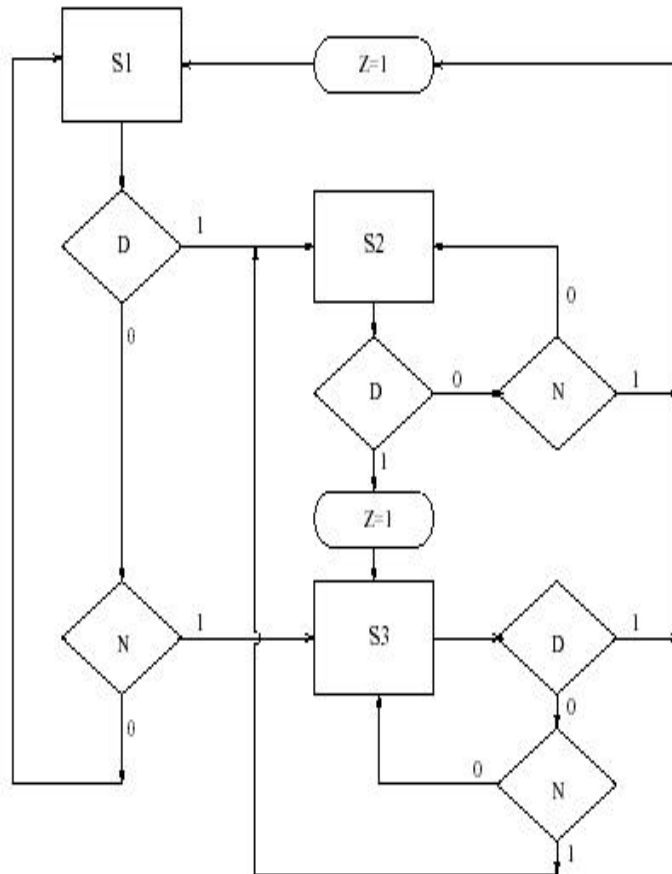
- a) Assume you have an integrated circuit chip that is 2cm x 2cm, the clock is generated in one corner of the chip, and the data from one flip-flop may have to be propagated to another, from any one place on the chip to any other.
- Draw a picture of the worst-case timing path between flip-flops.
 - What is the absolute minimum clock period?

Assume setup times of 0.1 ns, flip-flop propagation times of 0.2 ns, no other combinational logic in the paths and signal speed through circuit wires of $0.7c$ where c is the speed of light in a vacuum (300,000 kilometers / sec). You need not reduce the result to a single number. State any other assumptions made as part of your solution.

- b) **Briefly** describe a situation in which clock skew can be beneficial.

3) [12] The ASM chart below represents a finite state machine:

ASM chart



a) Is this a Moore or a Mealy machine?

b) What are the inputs and the outputs?

c) Draw a state diagram (with bubbles and arcs) for the machine

4) [20] ASM Charts

A serial input w comes into a computer at $1/3$ the system clock frequency. The input data is to be assembled by your circuit. The idle state of the input is high; the data received is 8 bits in length; the transmission begins with a low (start) bit, followed by the data LSB first, the rest of the data, and then a low (stop) bit. The circuit should provide an 8-bit output B and a done signal D .

a) Give pseudo-code for a solution to this problem

b) Draw an ASM chart for your pseudo-code

c) Show the data path circuit

d) Draw the ASM chart for the control circuit