University of Toronto

Department of Electrical and Computer Engineering

ECE 342 – Digital Hardware

Midterm Examination
March 2001

Last Name: _____

First Name: _____

Student #: _____

Signature: _____

Duration: **1.5 hours**

Answer ALL questions on this test paper.
There is extra space at the end if you need it.

Examiners Report

1	_____	**/15**
2	_____	**/10**
3	_____	**/15**
4	_____	**/10**
Total	_____	**/50**

Question 1 – [15 marks]

a. Assume we define the 2-cube A = x1x1, and also the 2-cubes B = xx11, C = x0x1, D = xx00, and E = x0x0. Consider the *-operations A* B, A * C, A * D, and A * E. Which of these operations produces as a result:

   i. A smaller cube: _____

   ii. A larger cube: _____

   iii. A 2 cube: _____

   iv. No cube (∅): _____

b. For the 2-cube A = x1x1, part a. above considered the *-operation with the 2-cubes B, C, D, and E. For this part, consider all possible 2-cubes. The *-operation of A with each of these possible 2-cubes would produce a resultant cube of a certain size. In the spaces below you are asked to give the total number of different 2-cubes for which the *-operation with A produces a cube of the specified size. Let the other cube in the *-operation be called Z:

   i. A * Z is (∅): # cubes = _____

   ii. A * Z is a 0-cube: # cubes = _____

   iii. A * Z is a 1-cube: # cubes = _____

   iv. A * Z is a 2-cube: # cubes = _____

   v. A * Z is a 3-cube: # cubes = _____

c. For a *k*-cube, answer the following:

   i. How many 0-cubes are contained in a *k*-cube: _____

   ii. How many (*k*-1)-cubes are contained in a *k*-cube: _____

d. Given

   C^{k+1} = { 0x1, x01, x11, 1x1, 11x } and
   G^{k+2} = { 001, 011, x1x, x11, 101, 1x1, 111 }

   Evaluate the following:

   $C^{k+2} = \{C^{k+1} \cup G^{k+2} - (\text{redundant cubes})\}$

   C^{k+2} = _____

Question 2 – [10 marks]

For a function, *f*, consider the following cover:

f (*x*1, *x*2, *x*3, *x*4, *x*5, *x*6) = {0x11x0, 0x111x, 01x011, 0x110x, 101111}

In the space below, you are to list the prime implicants of *f*. You must derive your answers in the space on the following page using the procedure discussed in class; specifically, you must use the procedure in which the original cover (given above) is called C^0 and you generate a new cover $C^1 = G^1 \cup C^0$ – (redundant cubes), and so on until the prime implicants are generated.

List the prime implicants below and derive them in the space given on the following page.

Prime implicants: _____

List the essential prime implicants (you do not have to show your derivation for this part):

_____

Derive the prime implicants in the space below:

Question 3 – [15 marks]

You are to design the circuit represented in Figure 1, which includes

- one 8-bit input register A, which contains a 2's complement signed number A {a7…a0}
- a FSM
- one 8-bit output register S, which contains a 2 complement signed number {s7…s0}

The FSM is used for a serial implementation of the operation S = -A (negation)

Hint: The 2'complement of a number A can be computed as the 1's complement +1

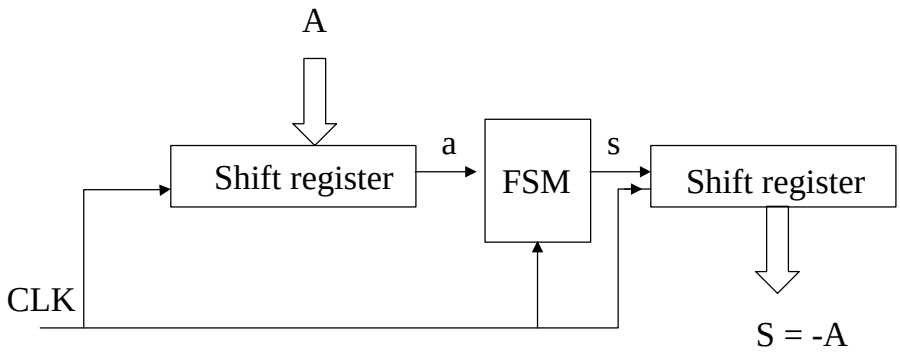


Figure 1

The shift registers have Enable and Load inputs.

a) Give the state diagram of the Mealy FSM that realizes the serial implementation of the negation operation. **[1 mark]**

b) Give the assigned state table of the Mealy FSM and the corresponding equations that are used to implement the FSM.
Use the standard notations : y_i for present states, Y_i for next states, a for the input and s for the output.

Assigned state table: **[1 mark]**

Equations: **[2 marks]**

c) Draw the Mealy FSM with D flip-flops (with Preset and Clear asynchronous inputs) and usual gates. **[1 mark]**

d) Give the state diagram of the Moore FSM that realizes the serial implementation of the negation operation. **[1 marks]**

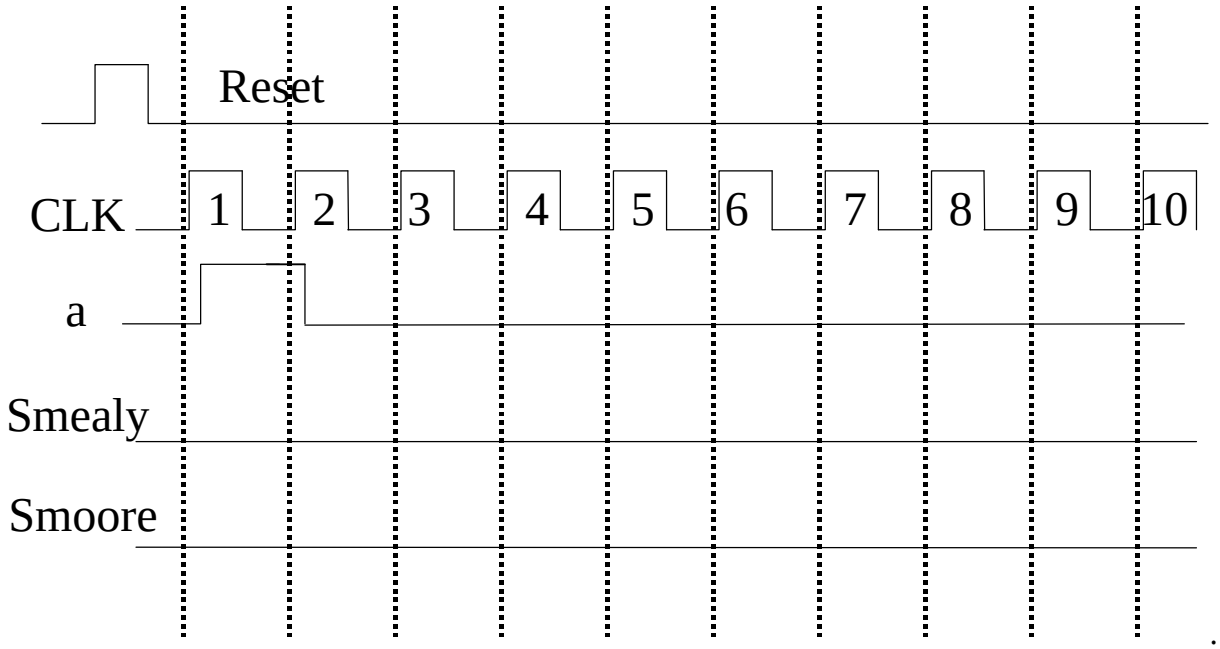
e) Give the assigned state table of the Moore FSM and the corresponding equations that are used to implement the FSM.
Use the standard notations : y_i for present states, Y_i for next states, a for the input and s for the output.

State assignment table **[1 mark]**

Equations: **[3 marks]**

f) Draw the Moore FSM with D flip-flops (with Preset and Clear asynchronous inputs) and usual gates. **[1 marks]**

g) Draw the outputs of the Mealy and Moore FSM corresponding timing diagram below
[2 marks]



h) Complete the circuit schematic of Figure 2. The input value is loaded in register A by the reset signal and the output value must be kept in the output register at the end of the operation. **[2 marks]**

Figure 2

Question 4 – [10 marks]

You are to design a circuit that produces the parity check bit of a n-bit word A by using the sequential approach. The parity bit is 1 when the n-bit word has an odd number of 1's. The parity bit is called p.

a) Write pseudo-code for the operation, using the format given in class. Assume A can be shift to the right. Try to use the algorithm that minimizes the circuit complexity, both for the data path and the control part. **[2 marks for optimal algorithm, 1 mark for non-optimal]**

b) Draw an ASM chart that represents your pseudo-code. Assume an externally supplied input ***s*** is provided and is set to 1 when A has been loaded and the operation should begin. Set an output ***Done*** to 1 when the operation is complete. **[2 marks]**

c) Draw a datapath for your circuit. Label all names with reasonable names. **[4 marks]**

d) For the control part, what would be the input and output signals? **[2 marks]**

Input signals:

Output signals:

Extra space. Use only if needed.

Extra space. Use only if needed.