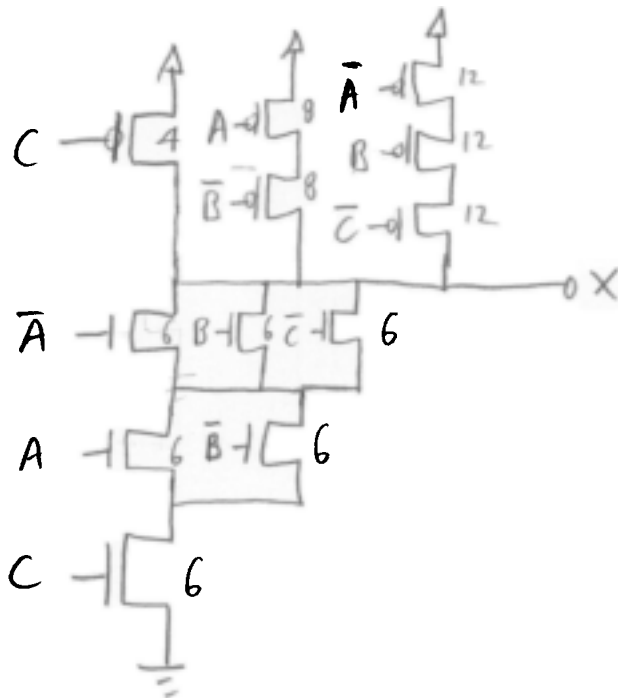


Name: SOLUTION Student No.: _____

1. Implement the equation $X = A\bar{B}C + \bar{A}B + \bar{C}$ using CMOS logic assuming that $A, \bar{A}, B, \bar{B}, C, \bar{C}$ are all available as inputs. Size the devices so that the output resistance is the same as that of an inverter with an NMOS $W/L=2$ and PMOS $W/L=4$ in worst case.

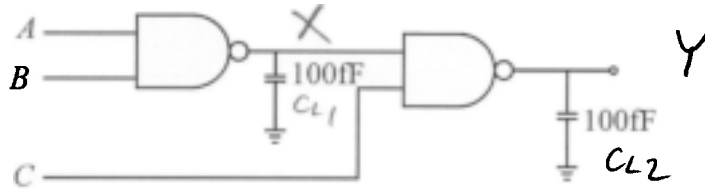
$$X = \overline{(\overline{A\bar{B}C})(\overline{\bar{A}B})(\bar{C})}$$

$$= (\bar{A} + B + \bar{C})(A + \bar{B})(C)$$



Name: SOLUTION Student No.: _____

2. Find the dynamic power dissipation for the following CMOS circuit assuming the clock is 1GHz, $V_{DD} = 2V$ and the inputs all are random values that change on the falling edge of the clock.



$$P_{X=0} = \frac{1}{4} \quad P_{X=1} = \frac{3}{4} \quad P_{X:0 \rightarrow 1} = \left(\frac{1}{4}\right)\left(\frac{3}{4}\right) = \frac{3}{16}$$

$$P_{Y=0} = P_{X=1} P_{C=1} = \left(\frac{3}{4}\right)\left(\frac{1}{2}\right) = \frac{3}{8}$$

$$P_{Y=1} = 1 - P_{Y=0} = \frac{5}{8} \quad P_{Y:0 \rightarrow 1} = \left(\frac{3}{8}\right)\left(\frac{5}{8}\right) = \frac{15}{64}$$

$$P_{DISS} = P_{X:0 \rightarrow 1} C_{L1} f_{CLK} V_{DD}^2 + P_{Y:0 \rightarrow 1} C_{L2} f_{CLK} V_{DD}^2$$

$$= \left(\frac{3}{16}\right)(100 \text{ fF})(1 \text{ GHz})(2^2) + \left(\frac{15}{64}\right)(100 \text{ fF})(1 \text{ GHz})(2^2)$$

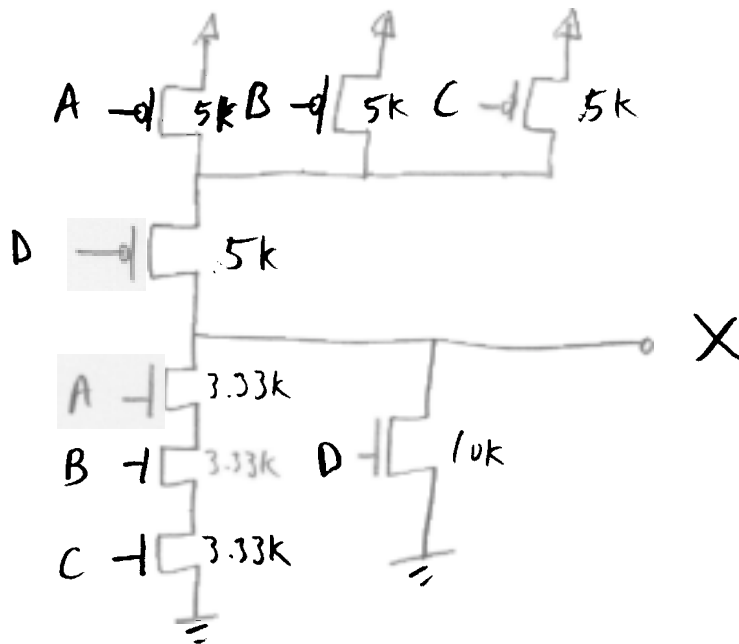
$$= \underline{\underline{169 \text{ } \mu\text{W}}}$$

Name: SOLUTION Student No.: _____

1. Implement the equation $X = (\bar{A} + \bar{B} + \bar{C})(\bar{D})$ using CMOS logic assuming that A, B, C, D are all available as inputs. Assume that the transistors have been sized to give an output resistance of 10k for the worst-case input pattern (in both the high output and low output cases). Find the input pattern that gives the lowest output resistance when the output is high. Also find the value of that resistance.

$$X = \overline{\bar{A} + \bar{B} + \bar{C}} + D$$

$$X = \overline{ABC} + D$$

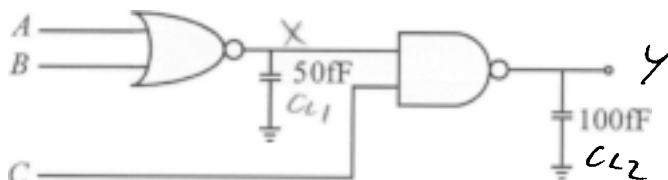


$A = B = C = D = 0$ IS LOWEST OUTPUT RESISTANCE
 & IT EQUALS $5k + 5k // 5k // 5k = 6.67k$

Name: SOLUTION Student No.: _____

2. Find the dynamic power dissipation for the following CMOS circuit assuming the clock is 1GHz, $V_{DD} = 2V$ and the inputs have the following probability values that change on the falling edge of the clock.

$$P(A=1) = 0.4, P(B=1) = 0.2, P(C=1) = 0.5$$



$$P_{X=1} = (0.6)(0.8) = 0.48 \quad P_{X=0} = 0.48 \quad 0.52$$

$$P_{X:0 \rightarrow 1} = (0.48)(0.52) = 0.2496$$

$$P_{Y=0} = P_{X=1} P_{C=1} = (0.48)(0.5) = 0.24$$

$$P_{Y=1} = 1 - 0.24 = 0.76$$

$$P_{Y:0 \rightarrow 1} = (0.24)(0.76) = 0.1824$$

$$\begin{aligned} P_{DISS} &= P_{X:0 \rightarrow 1} C_{L1} f_{CLK} V_{DD}^2 + P_{Y:0 \rightarrow 1} C_{L2} f_{CLK} V_{DD}^2 \\ &= (0.2496)(50\text{fF})(1\text{GHz})(2^2) + (0.1824)(100\text{fF})(1\text{GHz})(2^2) \\ &= \underline{\underline{123 \mu\text{W}}} \end{aligned}$$