

[5] Question 1:

a) When a NMOS transistor is in the “velocity saturation” region, what exactly is saturated?

The electrons velocity is saturated

b) Why is velocity saturation much more common in transistors with short channel lengths than transistors with long channel lengths?

Larger electric fields in short channel transistors

c) In a reverse biased pn junction, the depletion capacitance decreases as the reverse bias voltage is made larger. Does the stored charge in the depletion region **increase** or **decrease** as the reverse bias voltage is made larger?

The charge increases

d) When creating metal wiring on a microchip, which of the following 2 statements is true?

1) First, silicon dioxide is grown and photoresist is used to etch where wires should exist. Next, aluminum is sprayed on using silicon dioxide as a mask.

2) First, Aluminum is sprayed on the entire microchip, then photoresist and silicon oxide is used to mask where wires should exist and the rest is etched off.

#2

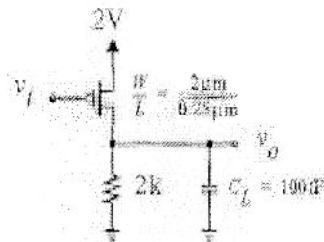
e) What is the processing step called when the wafer is heated to around 1000 degrees C and then slowly cooled?

Annealing

Last Name: MUSA

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[5] Question 2: For the inverter shown below, find t_{pHL} and t_{pLH} . Assume the input is a step change with low and high values of 0 and 2V. Also, assume the only capacitance in the circuit is the shown C_L .



$$t_{pHL} = 138 \text{ ps}$$

$$t_{pLH} = 97 \text{ ps}$$

$$t_{pHL} = 0.69 R_{eq} C_{eq} = 0.69 (2^k) (100^f) = 138 \text{ ps} \quad (2 \text{ marks})$$

$$t_{pLH} = 0.69 (R_{PMOS} \parallel 2^k) C_L = 0.69 (R_{PMOS} \parallel 2^k) (100^f)$$

$$R_{PMOS} = \frac{3}{4} \left(\frac{V_{DD}}{|I_{D,SAT}|} \right) \left(1 - \frac{5}{6} \left| \frac{V_{DSAT}}{V_{DD}} \right| \right)$$

$$I_{D,SAT} = k_p' \left(\frac{W}{L} \right) \left[(|V_{GS}| - V_{TH}) |V_{DSAT}| - \frac{1}{2} |V_{DSAT}|^2 \right]$$

$$= -30 \frac{\text{A}}{\text{V}^2} \left[(|10-2| - 1 \cdot 0.41) |1-1| - \frac{1}{2} |1-1|^2 \right]$$

$$= -264 \mu\text{A} = -0.264 \text{ mA}$$

$$R_{PMOS} = \frac{3}{4} \frac{2}{|-264 \times 10^{-3}|} \left(1 - \frac{5}{6} \left| \frac{0.1}{2} \right| \right) = 4.7^k$$

$$t_{pLH} = (0.69) (4.7 \parallel 2^k) (100^f) = 97 \text{ ps} \quad (3 \text{ marks})$$

[5] **Question 3:** Assuming velocity saturation does NOT occur, find the switching threshold, V_M , for an inverter where the NMOS has $W/L = 10$ and the PMOS has $W/L = 5$ and the power supply is 2V.

$$V_M = 0.74$$

From Equation Sheet:

$$V_M = (V_{Tn} + r(V_{DD} + V_{Tp})) / (1 + r) \quad (\text{sat})$$

$$r = \sqrt{-k_p / k_n} \quad (\text{sat})$$

Given (in equation sheet and question):

$$V_{DD} = 2V$$

$$V_{Tp} = -0.4V$$

$$V_{Tn} = 0.43V$$

$$k'_p = -30 \mu A / V^2$$

$$k'_n = 115 \mu A / V^2$$

$$(W/L)_p = 5$$

$$(W/L)_n = 10$$

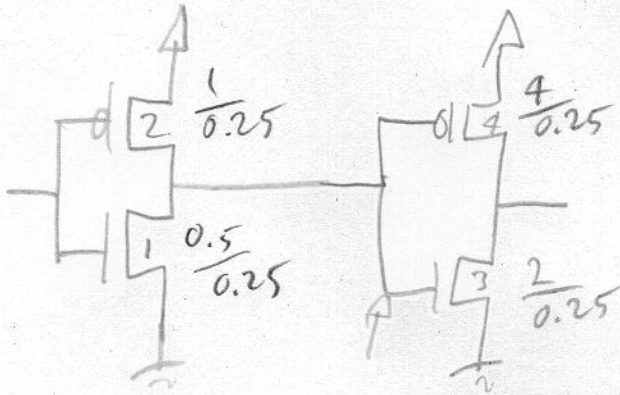
Solution:

$$r = \sqrt{\frac{-(W/L)_p k_p}{(W/L)_n k_n}} = \sqrt{\frac{5 * 30}{10 * 115}} = 0.361$$

$$V_M = (V_{Tn} + r(V_{DD} + V_{Tp})) / (1 + r) = (0.43 + 0.361(2 - 0.4)) / (1 + 0.361) = \underline{0.74V}$$

- [5] Question 4: A size 1 inverter has the NMOS size of $W/L = 0.5\mu\text{m}/0.25\mu\text{m}$ while the PMOS size is $W/L = 1\mu\text{m}/0.25\mu\text{m}$. Given that this size 1 inverter is driving a size 4 inverter (a fanout of 4), find the total effective load capacitance, C_L , at the output of the size 1 inverter IGNORING all drain-to-bulk capacitances and any wiring capacitance.

$$C_L = 11.55 \text{ fF}$$



FIND
 C_L AT THIS NODE

$$C_L = 2C_{gd1} + 2C_{gd2} + C_{gd3} + C_{gd4} + C_{g3} + C_{g4}$$

$$C_{gd1} = (C_{ox}) \times (W_1) = (0.31)(0.5) = 0.155 \text{ fF}$$

$$C_{gd2} = (0.27)(1) = 0.27 \text{ fF}$$

$$C_{gd3} = 4C_{gd1} = 0.62 \text{ fF}$$

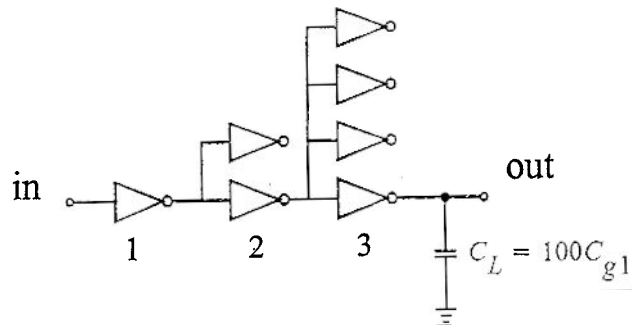
$$C_{gd4} = 4C_{gd2} = 1.08 \text{ fF}$$

$$C_{g3} = (W_3)(L_3)(C_{ox}) = (2)(0.25)(6) = 3 \text{ fF}$$

$$C_{g4} = (W_4)(L_4)(C_{ox}) = (4)(0.25)(6) = 6 \text{ fF}$$

$$C_L = 11.55 \text{ fF}$$

[5] **Question 5:** Consider the inverter tree shown below where all the second stage inverters are identical and all third stage inverters are identical. Find the relative sizing of the inverters to minimize the delay from input to output given that $C_L = 100C_{g1}$. C_{g1} is the input capacitance of the first stage inverter. (size i / size 1 is the relative size of inverter i to inverter 1).



$$\frac{\text{size 2}}{\text{size 1}} = 4.64$$

$$\frac{\text{size 3}}{\text{size 1}} = 10.77$$

$$\frac{2C_{g2}}{C_{g1}} = \frac{4C_{g3}}{C_{g2}} = \frac{C_L}{C_{g3}} = \frac{100C_{g1}}{C_{g3}}$$

$$A = \frac{C_{g2}}{C_{g1}} = \frac{\text{SIZE2}}{\text{SIZE1}}$$

$$B = \frac{C_{g3}}{C_{g1}} = \frac{\text{SIZE3}}{\text{SIZE1}}$$

$$\frac{2C_{g2}}{C_{g1}} = \frac{4C_{g3}}{C_{g2}} \Rightarrow 2A = 4\left(\frac{B}{A}\right) \Rightarrow A^2 = 2B$$

$$\frac{2C_{g2}}{C_{g1}} = \frac{100C_{g1}}{C_{g3}} \Rightarrow 2A = \frac{100}{B} \Rightarrow 2A = \frac{100}{A^2/2} \Rightarrow A^3 = 100$$

$$A = \sqrt[3]{100} = 4.64$$

$$B = A^2/2 = 10.77$$